

**Remarks/Arguments:**

Claims 1, 9-11, 16-18, 25-26, 33 and 34 are rejected. Claims 12-13 are allowed. Claims 1, 9, 18, 33 and 34 have been amended. No new matter has been added.

On page 2 the Advisory Action maintains the rejections based on the Inazumi reference. Specifically, on page 2 of the Official Action dated March 4, 2009, claims 1, 9-11, 16-18, 25-26 and 33-34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumi (U.S. Patent 6,038,094) in view of Shinohara (U.S. Patent 5,740,306) and further in view of Inazumi (U.S. Patent 6,493,362). It is respectfully submitted, however, that the claims are patentable over the art of record for at least the reasons set forth below.

Applicants' invention, as recited by claim 1, includes features which are neither disclosed nor suggested by the art of record, namely:

**... detecting a data rate of the received bit stream by counting a number of packets received by said inputting means at intervals of a predetermined time period ...**

Claim 1 relates to detecting a data rate of an input bit stream. Specifically, the number of packets in the stream are counted at intervals of time. Support for these features can be found on at least page 34, line 10 to page 35, line 5, of Applicants' specification and furthermore in Figs. 1 and 5b. No new matter has been added.

In Column 4, lines 38-63, Inazumi suggests that a preset time value T is computed based on the counted number of packets and the bit rate ("*T is calculated in the generating step by using a number of packets N ... the length L of those packets ... and the bit rate R*"). Specifically, the PCR value T is also described in Column 9, lines 25-55 of Inazumi ("*calculates a new PCR value T ... N is the number of packets counted ... bit rate R*"). Inazumi's bit rate of the received bit stream, however, is not detected based on the counted number of packets. Specifically, Inazumi's bit rate R for recording/reproducing is set based on the divided clock frequency as described in Column 5, lines 15-25, Column 8, lines 20-40, and Column 9, lines 45-55 ("*the bit rate R may be whatever desired value it permits extraction of a desired program data ... that is, the bit rate R may be set arbitrarily ... here, the recording or reproducing bit rate R of the data recording/reproducing unit 100 is set based on the internal clock signal outputted from the frequency divider 25 to the PCR generating section 17*"). Specifically, Inazumi's

frequency divider 25 divides the reference clock signal outputted from clock oscillator 24 and generates the internal clock signal to be used for the recording/reproducing bit rate R (not the bit rate of the received bit stream).

On page 2, the Advisory Action suggests that Inazumi's PCR value is computed based on the counted number of packets and then the PCR determines the bit rate of the received bit stream. Applicants, however, respectfully disagree. Specifically, Inazumi teaches that the value T is computed based on the bit rate R of recording/reproducing the stream (not the bit rate of the received bit stream). Thus, the PCR value T is determined based on the counted number of packets, and is used to calibrate the reference clock signal which is divided and utilized for recording/reproducing the stream. For example, as stated in column 8 of Inazumi, if the bit rate of the received bit stream is 4.7MHz, the frequency divider divides the 27MHz reference clock signal to produce a 5.0625MHz internal clock signal which is set as recording/reproducing bit rate R (recording/reproducing bit rate R (5.0625MHz) is computed based on the counted number of packets; the bit rate (4.7MHz) of the received bit stream is not computed based on the counted number of packets).

Applicants' claim 1 is different than the art of record, because the data rate R is detected based on counting the number of packets at intervals of a predetermined time ("*detecting a data rate of the received bit stream by counting a number of packets received by said inputting means at intervals of a predetermined time period*"). As shown in Applicants' Figs. 8a and 8b, the data rate of the received bit stream may fluctuate over time. Thus, the packet counter 16 and bit rate calculator 20 as shown in Fig. 5b are able to detect the bit rate R of the received bit stream over an interval of predetermined time. For example, as described on pages 34 and 35 of the specification, the bit rate calculator 20 is able to calculate the bit rate R based on a number of packets counted over a time period ("*calculating circuit 20 calculates the bit rate of input packets ... output of the counter value holding circuit 17 is N ... time period for one track is a time T ... data mount per packet is D ...  $R = (D \times 8 \times N)/T$* "). Thus, the number of packets N are counted over an interval of time T.


Neither Shinohara nor Matsumi suggests the features of amended claim 1. Thus, the combination of Matsumi, Shinohara and Inazumi is deficient in teaching Applicants' claim 1. Accordingly, for the reasons set forth above, claim 1 is patentable over the art of record.

Independent claims 18, 33 and 34 have similar features of claim 1. Thus, claims 18, 33 and 34 are also patentable over the art of record for the reasons set forth above.

Dependent claims 9-13, 16-17 and 25-26 include all the features from the claims from which they depend. Thus, these claims are also patentable over the art of record for at least the reasons set forth above.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,



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